In the claims:

Claims 1 to 22 (canceled)

23. (previously presented) A computer-implemented method for modeling a high-performance, high I/O ball grid array substrate, intended for integrated circuit flip-chip assembly and having a first and a second metal layer and one intermediate insulating layer, all of substantially equal areas, comprising the steps of:

modeling the structure of said first metal layer as electrical ground potential, said layer having a plurality of electrically insulated openings for electrical contacts;

modeling the structure of said second metal layer as a plurality of electrical signal lines, a plurality of first electrical power lines operable at a first potential, and a plurality of second electrical power lines operable at a second potential;

configuring said first power lines so wide that their combined inductances approximate the inductance of a metal having the size of the total substrate;

concurrently distributing said first power lines among said signal lines in order to provide at least minimum inductive coupling between signal and power lines, thereby obtaining high mutual inductances and minimizing effective self-inductance;

configuring said second power lines to serve as distributed areas having wide geometries for minimizing self-inductance and merging into a central area supporting said chip; and

modeling the structure of said insulating layer for positioning it between said first and second metal layers, and selecting its thickness and material characteristics suitable for strong electromagnetical coupling between said signal lines and said first metal layer, thereby providing a predetermined impedance to ground and minimizing cross-talk between signal lines.

24. (previously presented) A method for fabricating a high performance, high I/O ball grid array substrate, intended for two patterned metal layers and integrated circuit flip-chip assembly, comprising the steps of:

providing an electrically insulating layer having a first and a second surface;

forming a plurality of via holes in said insulating layer and filling said holes with electrically conductive material;

attaching one of said metal layers to said first surface, said metal layer intended to provide electrical ground potential;

forming a plurality of electrically insulated openings in said metal layer, said openings intended for outside electrical contacts;

attaching the other of said metal layers to said second surface, said metal layer intended to provide electrical signal and power potentials;

configuring portions of said metal layer as a plurality of electrical signal lines, further portions as a plurality of first electrical power lines, and further portions as a plurality of second electrical power lines, thereby creating contact between selected signal and power lines and said vias;

forming an insulating protective film over the exposed surface of said ground layer, and an insulating film over the exposed surfaces of said signal and power lines; and

forming pluralities of openings in both said insulating films, and filling said openings with solderable metal, thereby creating attachment sites for outside solder balls and for chip solder bumps.

25. (previously presented) The method according to Claim 24 further comprising the step of attaching an integrated circuit chip, having an active surface including solder bumps, by adhering said solder bumps to said plurality of metal-filled openings in said outermost insulating film protecting said signal and power lines.

26. (previously presented) The method according to Claim 25 further comprising the step of filling with a polymeric encapsulant any gaps between said substrate and said chip left void after said chip solder bumps are adhered to said plurality of openings in said outermost insulating film protecting said signal and power lines.

27. (previously presented) The method according to Claim 24 further comprising the step of surrounding said chip with a polymeric encapsulation compound.

28. (previously presented) The method according to Claim 27 further comprising the step of attaching a heat spreader positioned on the outer surface of said encapsulation material.

29. (previously presented) The method according to Claim 24 further comprising the step of attaching solder balls to said plurality of metal-filled openings in said outermost insulating film protecting said ground layer.

Claim 30 (new) A method of fabricating a packaged integrated circuit, comprising the steps of:

providing a substrate having first and second opposing surfaces;

providing a plurality of signal lines, a plurality of first power lines coupleable to a first power source, and a plurality of second power lines coupleable to a second power source, all on said second surface, at least one of said plurality of signal lines disposed ~~is~~ between a pair of said plurality of first power lines, and said signal lines between said pair of said plurality of first power lines and said pair of said plurality of first power lines disposed ~~are~~ between a pair of said second power lines; and

providing an integrated circuit chip mounted on said substrate.

Claim 31 (new) The method of Claim 30, further including providing said signal lines of a first width, said first power lines of a second width different from said first, and said second power lines of a third width different from said first and second widths.

Claim 32 (new) The method of Claim 31, wherein said third width is wider than said second width, and said second width is wider than said first width.

Claim 33 (new) The method of Claim 30, further including the step of providing a ground plane on said first surface of said substrate.

Claim 34 (new) A method of fabricating a packaged integrated circuit, comprising the steps of:

providing a substrate having first and second opposing surfaces, said substrate having thereon:

providing a plurality of groups of lines, said plurality of groups of lines including groups of lines of at least three different widths disposed on said second surface of said substrate, said groups of lines arranged such that one or more lines in a first group of lines of a first width are disposed between lines of a second group of lines of a second width and lines in a said second group of lines of said second width are disposed between lines of said third width; and

providing an integrated circuit chip;

mounting said chip on said substrate; and

coupling said chip to at least some of said lines.

Claim 35 (new) The method of Claim 34, wherein said lines of said first width are signal lines, said lines of said second width are power lines coupled to a first voltage potential, and said lines of said third width are power lines coupled to a second voltage potential.

Claim 36 (new) The method of Claim 34, further comprising the step of providing a ground plane on said first surface of said substrate.